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PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Steven R. Fox, et al.

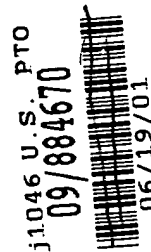
Docket: YOR920010104US1(14270)

Serial No.: Unassigned

Dated: June 19, 2001

Filed: Herewith

For: DIVOT REDUCTION IN SIMOX LAYERS



Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. U.S. Patent No. 6,090,689, issued July 18, 2000 to Sadana, et al.
2. U.S. Patent No. 6,043,166, issued March 28, 2000 to Roitman, et al.;
3. U.S. Patent No. 5,930,643, issued July 27, 1999 to Sadana, et al.;
4. U.S. Patent No. 5,589,407, issued December 31, 1996 to Meyappan, et al.;

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

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I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to the Assistant Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Dated: June 19, 2001


Michelle Mustafa

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5. U.S. Patent No. 5,519,336, issued May 21, 1996 to Liu, et al.;
6. U.S. Patent No. 5,288,650, issued February 22, 1994 to Sandow;
7. U.S. Patent No. 5,279,978, issued January 18, 1994 to See, et al.;
8. U.S. Patent No. 4,975,126, issued December 4, 1990 to Margail, et al.;
9. U.S. Patent No. 4,902,642, issued February 20, 1990 to Mao, et al.;
10. U.S. Patent No. 4,786,608, issued November 22, 1988 to Griffith;
11. U.S. Patent No. 4,749,660, issued June 7, 1988 to Short, et al.;
12. Abstract of Japanese Patent No. JP 63 217657, issued September 9, 1988;
13. Wolf, S., "Silicon Processing for the VLSI ERA", Vol. 2: Process Integration, 1990, pp. 72-73; and
14. White, A.E., et al., "The role of implant temperature in the formation of thin buried oxide layers", BEAM-SOLID INTERACTIONS AND TRANSIENT PROCESSES SYMPOSIUM, BOSTON, MA, USA, 1-4 DEC. 1986, pp. 585-590, XP000922701.

Applicants are submitting copies of the above-cited references.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. §1.97(b), no petition, certification or fee is required.

Respectfully submitted,



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INFORMATION DISCLOSURE CITATION*(Use several sheets if necessary)*

Docket Number (Optional)

YOR920010104US (4370)

Application Number

Unassigned

Applicant(s)

Steven R. Fox, et al.

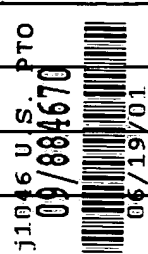
Filing Date

Herewith

Group Art Unit

Unassigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,090,689	07/18/00	Sadana, et al.			
		6,043,166	03/28/00	Roitman, et al.			
		5,930,643	07/27/99	Sadana, et al.			
		5,589,407	12/31/96	Meyappan, et al.			
		5,519,336	05/21/96	Liu, et al.			
		5,288,650	02/22/94	Sadow			
		5,279,978	01/18/94	See, et al.			
		4,975,126	12/04/90	Margail, et al.			
		4,902,642	02/20/90	Mao, et al.			
		4,786,608	11/22/88	Griffith			
		4,749,660	06/07/88	Short, et al.			

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
		JP 63 217657	09/09/88	Japan				

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Wolf, S., "Silicon Processing for the VLSI ERA", Vol. 2: Process Integration, 1990, pp. 72-73
		White, A.E., et al., "The role of implant temperature in the formation of thin buried oxide layers", BEAM-SOLID INTERACTIONS AND TRANSIENT PROCESSES SYMPOSIUM, BOSTON, MA, USA, 1-4 DEC. 1986, pp. 585-590, XP000922701

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.